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Description

VARIATION OF EFFECTIVE FILTER CAPACITANCE IN PHASE LOCK LOOP CIRCUIT LOOP FILTERS

Background of Invention

[0001] 1. Technical Field

[0002] The present invention relates to a structure and associated method to vary an effective capacitance in a phase lock loop circuit comprising a loop filter.

[0003] 2. Related Art

[0004] Parameters of electrical circuits typically require optimization. An electrical circuit comprising parameters that are not optimized may not perform efficiently and therefore may malfunction. Therefore there exists a need to optimize parameters of electrical circuits.

Summary of Invention

[0005] The present invention provides a phase lock loop circuit, comprising:

[0006] a first charge pump circuit, a second charge pump circuit, and a loop filter circuit within the phase lock loop circuit, the loop filter circuit comprising a filter capacitor with a constant capacitance value, the first charge pump circuit being electrically connected to the loop filter, the first charge pump circuit being adapted to control a flow of current for the loop filter, the loop filter being adapted to provide a voltage for a voltage controlled oscillator, the second charge pump circuit being electrically connected to the loop filter circuit in parallel with the filter capacitor, and the first charge pump circuit and the second charge pump circuit being adapted to collectively vary an effective capacitance value of the filter capacitor.

[0007] The present invention provides a method for optimizing a phase lock loop circuit, comprising:

[0008] providing a first charge pump circuit, a second charge pump circuit, and a loop filter circuit within the phase lock loop circuit, the loop filter circuit comprising a filter capacitor with a constant capacitance value, the first charge pump circuit being electrically connected to the loop filter, and the second charge pump circuit being electrically connected to the loop filter circuit in parallel with the filter capacitor;

[0009] controlling, by the first charge pump circuit, a flow of current for the loop filter;

[0010] varying, by the first the first charge pump circuit and the second charge pump circuit, an effective capacitance value of the filter capacitor; and

[0011] providing, by the loop filter, a voltage for a voltage controlled oscillator.

[0012] The present invention advantageously provides a structure and associated method to optimize parameters of electrical circuits.

Brief Description of Drawings

[0013] FIG. 1 illustrates a block diagram view of a phase lock loop (PLL) circuit, in accordance with embodiments of the present invention.

[0014] FIG. 2 illustrates a schematic of the loop filter circuit in FIG. 1 in relation to the main charge pump circuit and the auxiliary charge pump circuit, in accordance with embodiments of the present invention.

[0015] FIG. 3 illustrates a graph of a gain verses a frequency for the phase lock loop circuit 1 of FIG. 1, in accordance with embodiments of the present invention.

[0016] FIG. 4 illustrates a graph of a gain verses a frequency for the phase lock loop circuit 1 of FIG. 1 with the peaking ef-

fect of FIG. 3 removed, in accordance with embodiments of the present invention.

[0017] FIG. 5 illustrates a graph showing an effect of an abrupt change to an input frequency, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION

[0018] FIG. 1 illustrates a block diagram view of a phase lock loop (PLL) circuit 1 comprising a phase detector 22, a loop filter circuit 2, a main charge pump circuit 5, an auxiliary charge pump circuit 8, and a voltage controlled oscillator (VCO) 11, in accordance with embodiments of the present invention. The phase detector 22 compares a phase and frequency of a reference signal 8 to a phase and frequency of a feedback signal 10 from the VCO 11. The phase detector 22 generates an error signal 29 representing the phase and frequency difference between the reference signal 8 and the feedback signal 10. The error signal 29 is transmitted to the main charge pump circuit 5 and the auxiliary charge pump circuit 8. Based on the error signal 29, the main charge pump circuit 5, the auxiliary charge pump circuit 8, and the loop filter circuit 2 collectively produce a correction signal 32 that controls the VCO to produce an output signal 24 that tracks the reference

signal 8 (i.e., output signal 24 tracks a phase and frequency of the reference signal 8). The feedback signal 10 is equivalent to or a sample of the output signal 24. A relationship between the main charge pump circuit 5, the auxiliary charge pump circuit 8, and the loop filter circuit 2 is described in detail in the description of FIG. 2, infra.

[0019] FIG. 2 illustrates a schematic of the loop filter circuit 2 in relation to the main charge pump circuit 5 and the auxiliary charge pump circuit 8, in accordance with embodiments of the present invention. The loop filter circuit 2 comprises a first capacitor 4, a second capacitor 18 (e.g., filter capacitor), and a resistor 12. The first capacitor 4 is electrically connected to the resistor 12. The resistor 12 is electrically connected to the second capacitor 18. The first capacitor 4 is in parallel with the resistor 12 and the second capacitor 18. The resistor 12 comprises a fixed resistance R_1. The first capacitor 4 comprises a fixed capacitance C_1. The second capacitor 18 comprises a fixed capacitance C_2. The main charge pump circuit 5 may inject (i.e., source) current to the loop filter circuit 2. Alternatively, the main charge pump circuit 5 may remove (i.e., sink) current from the loop filter circuit 2. The source or sink function of the main charge pump circuit 5 may be

controlled by a user. The auxiliary charge pump circuit 8 is electrically connected to the loop filter circuit 2 in parallel with the second capacitor 18. The auxiliary charge pump circuit 8 may inject (i.e., source) current to the second capacitor 18. Alternatively, the auxiliary charge pump circuit 8 may remove (i.e., sink) current from the 2 second capacitor 18. The source or sink function of the auxiliary charge pump circuit 8 may be controlled by the user. The main charge pump circuit 5 may comprise an adjustable gain control so that the user may vary a current gain of the main charge pump circuit 5 (G_m). The auxiliary charge pump circuit 8 may comprise an adjustable gain control so that the user may vary a current gain of the main charge pump circuit 5 (G_a). By changing the current gain G_a of the auxiliary charge pump circuit 8 in relation to the current gain G_m of the main charge pump circuit 5, an effective capacitance value of the second capacitor 18 (C_{eff}) may be controlled. The effective capacitance value C_{eff} is a value of capacitance that thethe second capacitor 18 appears to have. Although the second capacitor 18 comprises the fixed capacitance value C_2, the effective capacitance C_{eff} value is higher or lower than the fixed capacitance value C_2. By changing both gains G_a and G_m relative

to each other, a wide range of effective capacitance values C_{eff} for the second capacitor 18 is obtained. When the main charge pump circuit 5 and the auxiliary charge pump circuit 8 both flow current in a same direction (i.e., the main charge pump circuit 5 and the auxiliary charge pump circuit 8 both sink current or both source current), a value for C_{eff} is determined by the following first equation: $C_{eff} = (C_2 * G_m)/(G_m + G_a)$. Using the first equation, C_{eff} decreases as G_a increases. When the main charge pump circuit 5 and the auxiliary charge pump circuit 8 each flow current in opposite directions (i.e., the main charge pump circuit 5 sinks current and the auxiliary charge pump circuit 8 sources current or vice versa), a value for C_{eff} is determined by the following second equation: $C_{eff} = (C_2 * G_m)/(G_m - G_a)$ with a limitation that $G_a < G_m$. Using the second equation, C_{eff} increases as G_a increases. It is readily apparent that if both G_m and G_a are varied, then C_{eff} can be varied over a wider range then if just G_m or G_a is varied. For example, if $G_m = 1$, $G_a = .5$, and $C_2 = 350$ picofarads (pF) then using the first equation produces a C_{eff} of 233pF and using the second equation produces a C_{eff} of 700pF thereby giving C_{eff} a range of 233pF-700pF. The variation of C_{eff} allows for optimization of phase lock loop

circuit 1 parameters such as, inter alia, bandwidth, peaking/damping factor (ζ), noise reduction, etc. A relationship between the damping factor ζ and C_{eff} and is shown by the following equation:

[0020] $$\zeta = (R_1 / 2) * \sqrt{(G_m * I_{ref} * K_1 * C_{eff}) / 1}$$

[0021] The current value I_{ref} in the preceding equation is a reference current applied to the phase lock loop circuit 1. The value K_1 in the preceding equation is a DC portion of a gain of the VCO 11.

[0022] As shown by the preceding equation, the damping factor ζ goes up as C_{eff} is increased. A higher damping factor allows the phase lock loop circuit 1 to respond to an abrupt change in the input signal frequency without excessive overshooting (e.g., see FIG. 5). A bandwidth of the phase lock loop circuit 1 is defined as a frequency at which a closed loop gain G_{cl} of the phase lock loop circuit 1 is equal to -3 decibels (db). The closed loop gain G_{cl} of the phase lock loop circuit 1 is shown by the following formula:

[0023] $$G_{cl} = (G_m * I_{ref} * K_1 * (s + \omega_z)) / (s^3 * C_2 + s^2 * C_2 * \omega_{p+} G_m * I_{ref} * K_1 * (s + \omega_z))$$

[0024] The symbol s represents the Laplace transform operator.

The value $\omega_z = 1/(R_1 * C_{eff})$. The value $\omega_p = 1/(R_1 * C_2)$. Therefore, because the bandwidth is related to the closed loop gain G_{cl} and the closed loop gain G_{cl} is dependent upon C_{eff} (see $\omega_z = 1/(R_1 * C_{eff})$), it is evident that a variation of C_{eff} will vary the the phase lock loop circuit 1 bandwidth. A wide range of C_{eff} allows for a wide range of bandwidth for the phase lock loop circuit 1. Varying the bandwidth and damping factor for the phase lock loop circuit 1 allows for the rejection of noise (i.e., electrical noise) to the phase lock loop circuit 1 and therefore is a method of noise reduction. More than one phase lock loop circuit 1 parameter may varying simultaneously. For example, the bandwidth and damping factor for the phase lock loop circuit 1 may be varyed simultaneously. Examples of the effects of optimization of a damping factor of the phase lock loop circuit 1 are described in FIGS 3, 4, and 5.

[0025] FIG. 3 illustrates a graph of a gain from the input reference signal 8 to the output signal 24 from the VCO verses frequency for the phase lock loop circuit 1 of FIG. 1, in accordance with embodiments of the present invention. The X-axis represents the frequency in hertz (Hz) for the phase lock loop circuit 1. The Y-axis represents the mag-

nitude of the gain in decibels (dB). A value of C_{eff} has been set to 116 pF. It can be seen on the graph of FIG. 3 that the gain has a peaking effect 42 starting at about 10^5 Hz (i.e., magnitude slightly rising from about 14 dB to about 17 dB). The peaking effect 42 has the tendency of amplifying any electrical noise that may be part of the input reference signal 8 thus causing excessive noise on the output signal 24. The peaking effect 42 is caused by the damping factor ζ (see description of FIG. 2) being less than optimum, thereby causing the phase lock loop circuit 1 to be underdamped. The peaking effect 42 is removed in FIG. 4by changing the value of C_{eff} as described infra.

[0026] FIG. 4 illustrates a graph of a gain from the input reference signal 8 to the output signal 24 from the VCO verses frequency for the phase lock loop circuit 1 of FIG. 1 with the peaking effect 42 of FIG. 3 removed, in accordance with embodiments of the present invention. The X-axis represents the frequency in hertz (Hz). The Y-axis represents the magnitude of the gain in decibels (dB). A value of C_{eff} has been set to 700 pF. It can be seen on the graph of FIG. 4 that the the peaking effect 42 of FIG. 3 has been removed and the magnitude of the gain comprises a steady value of about 14 dB. Therefore the damping factor

for the phase lock loop circuit 1 has been optimized by changing the value of C_{eff} thereby causing the phase lock loop circuit 1 to be properly damped.

[0027] FIG. 5 illustrates a graph showing an effect on a frequency of the output signal 24 by abruptly changing a frequency of the input reference signal 8 for the phase lock loop circuit 1 of FIG. 1, in accordance with embodiments of the present invention. The Y-axis represents the frequency of the output signal 24 in kilohertz. The X-axis represents time in nanoseconds. The plots 50 and 52 both show a response of the output signal 24 frequency to an abrupt change of the input clock frequency of the input reference signal 8. For the plot 50, the auxiliary charge pump 8 has been turned off and therefore $G_a=0$ and $C_{eff} = C_2$. Due to the abrupt change in the input clock frequency, the plot 50 shows an under damped oscillatory response of the the output signal 24 frequency. The output signal 24 frequency does not stop oscillating until about 14 nanoseconds. The plot 52 shows the effect that increasing C_{eff} (i.e., the auxiliary charge pump 8 has been turned back on for the same abrupt change in the input clock frequency of the input reference signal 8 for the plot 50) has on the oscillation of the output signal 24 frequency during the

abrupt change of frequencies. As shown by the plot 52, there is very little oscillation during the abrupt change of frequencies thereby causing a more damped response to the abrupt change in frequencies than the plot 50. It is readily apparent that by increasing C_{eff} the damping factor is increased and therefore the plot 52 recovers from oscillation quicker than the plot 50.

[0028] While embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.